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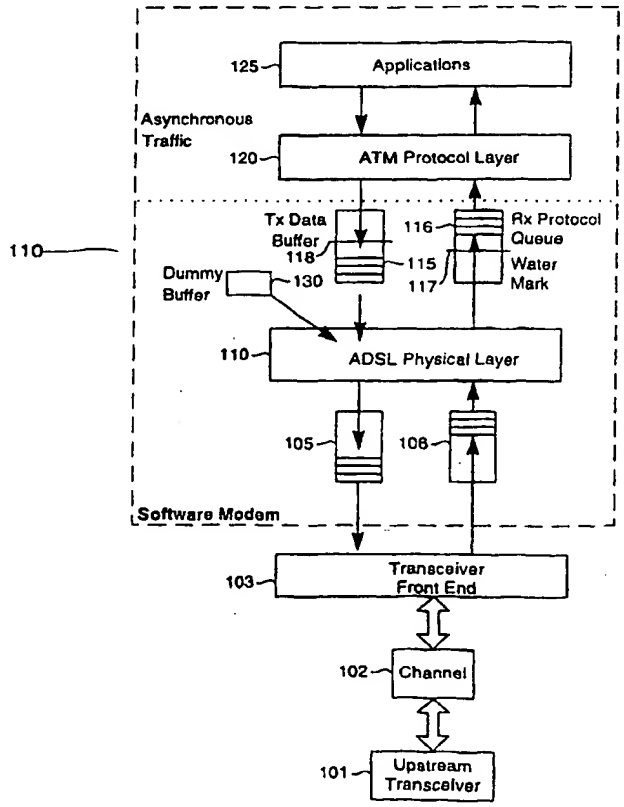
(54) Title: SYSTEM AND METHOD FOR REDUCING LATENCY IN SOFTWARE MODEM FOR HIGH–SPEED SYNCHRONOUS TRANSMISSION

(57) Abstract

An ADSL physical transmission layer (110) retrieves data to be transmitted from either a transmit data buffer (115), or a dummy cell buffer (130) in the case when no actual data is being transmitted to maintain a continuous data stream in an ADSL data link. The ADSL physical transmission layer (110) and an associated ATM protocol layer (120) are implemented as an interrupt service routine and delayed procedure call respectively in an ADSL software modem application. Because the ATM protocol layer (120) does not fill the transmit data buffer (115) with dummy cell data, it is simpler and faster. Moreover, latency is minimized, and overall system throughput enhanced since the maximum latency is independent of any operating system latency, and is no greater than the size of the cell stored in the dummy cell buffer (130). The invention has significant potential for performance and latency of computing systems pose engineering challenges in maintaining a continuous data link between a real time transceiver and a non–real time operating system.



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SYSTEM AND METHOD FOR REDUCING LATENCY IN SOFTWARE MODEM FOR HIGH-SPEED SYNCHRONOUS TRANSMISSION

FIELD OF THE INVENTION

The invention relates generally to asynchronous data transfer over a high-speed synchronous transmission system, such as those utilizing ATM transport over a Digital Subscriber Line (DSL). More particularly, the present invention is directed to latency minimization between a host computing system and an ADSL transceiver.

BACKGROUND OF THE INVENTION

In a high-speed synchronous transmission system, modulated symbols are sent continuously in time. When it is implemented by a computer host processor (so called software modem), it is extremely critical to maintain a continuous bit stream output between the real time transceiver and the non-real time host system (such as a local host computing system running an operating system such as Microsoft Windows® NT or the like). To reduce transport delay, latencies between each interface located in the data path (i.e., between the upstream transceiver to operating system) must be kept to a minimum.

There are a number of such interfaces in such data path, and various mechanisms have been proposed to ensure a continuous stream of demodulated/modulated data. First, an analog channel interface portion of a downstream ADSL transceiver is responsible for receiving, transmitting, processing analog data signals, and maintaining a synchronized data link through a channel to an upstream transceiver interface. This is a real-time link, and accordingly a modulated signal must be present (at some level, even in reduced power management modes) at all times. An example of a prior art approach for ensuring that the data link is kept synchronized, even when one end is connected to an asynchronous source, is U.S. Patent No. 5,003,558. This reference teaches sending an "idle" signal to keep the link active even when there is no real data, but, notably, does not address the problem of how to cure latencies which may be present in such asynchronous source.

Next after the channel interface portion in the data path lies a physical layer

transport circuit. This portion of the data link is responsible for modulating and demodulating data symbols. To reduce latencies between the channel interface and the physical layer, Receive/Transmit FIFO buffers are used. This technique is well known in the art, and an example of this type of technology is depicted in U.S. Patent Nos. 4,823,312 and 5,140,679 assigned to National. Accordingly, there are reasonably well developed solutions to the problems of latency and transport delay between a channel interface and physical layer in an ADSL transceiver, and this portion of the data path can be maintained as real time without undue cost and/or complexity.

A larger challenge is posed, however, by the data path located between the physical layer and the logical layer, in this case, an ATM protocol layer. The ATM protocol layer is required to interface both with the physical layer (a real time data path) and with the operating system (an asynchronous data path). To reduce latencies between these two interfaces, one approach would be to use the same kinds of Receive/Transmit FIFO buffers as explained earlier between the channel interface and physical layer. In this respect, on the receive side of the data path, it is possible to use a sufficiently large Receiver buffer to compensate for latencies inherent in the operations of the ADSL physical layer and ATM protocol layer when the latter are implemented in a software modem. Such latencies arise from the fact that, in a software modem context, both such functions are performed by the host processing device executing routines of different priority. For instance, in a Windows operating system, the ADSL physical layer is configured as an Interrupt Service Routine (ISR), while the ATM protocol layer is set up as a lower priority Delayed Procedure Call (DPC). The ADSL Physical layer is configured as a high priority task in the operating system, because, in this manner, latency between this layer and the channel interface is reduced, and the buffers between such interfaces can be reduced as well.

Because a DPC is a lower priority task than an ISR, however, there is an inherent latency between the physical layer and ATM operations, and a Receiver buffer must be employed between the two to handle such disparity. Nevertheless, when a buffer is used, a transport delay is introduced, which, of course, is undesirable. To reduce this delay, the buffer size must be correspondingly reduced. This design goal of course must be tempered by the fact that the buffer must be at least large enough to accommodate expected latencies caused by the difference in priorities of

the ADSL Physical Layer and the ATM protocol layer. One proposed solution would be to make the ATM protocol an ISR as well, so that there is no latency between the ADSL Physical Layer and the ATM protocols. This approach is unattractive for the plain fact that ATM protocols require many system calls that cannot be accommodated in an ISR routine, because such routines must be executed in a very short period of time.

Consequently, in most ADSL software modem systems, it is expected there will be a buffer interface between the ADSL physical layer and the ATM protocol. The size of the buffer can be varied, of course, depending on the expected channel data rate, expected operating system latencies, etc. In a typical PC using Microsoft Windows, a latency time of about 10 to 30 msec is contemplated. It is, of course, extremely critical to reduce this latency as much as possible to ensure efficient data transmissions across the entire data link.

One approach suggested in the prior art (such as described in the aforementioned references above) is to include some kind of threshold fill point, or "water mark" for the receive and transmit buffers. In the transmit direction, a transmit buffer water mark is set to some value that is close to the full capacity of the buffer size. When the data in the buffer drops below this mark, an ATM protocol layer routine is activated and more data is loaded (poured in) in the transmit buffer. Accordingly, at any moment in time, an amount of data equal to the transmit buffer water mark level is available to sustain continuous data transmission due to system latency. In the receiving direction, a receive buffer water mark is set to some value close to the empty capacity of the buffer size. When the buffer fills with data above this level, the ATM protocol layer routine is again activated and more data is extracted (poured out) from the receive buffer. Accordingly, at any moment in time, an amount of data equal to the capacity above the receive water mark level is available for the synchronous receiver to store received data due to system latency.

The problem with this approach is the fact that there is often no real data to be transmitted by the operating system to the upstream transmitter, yet the data link on the upstream side must be maintained. As a result, after verifying from the operating system that there are no applications transmitting data, the ATM protocol layer routine must load the buffer with "dummy" data corresponding to a fixed pattern recognizable by the upstream transmitter as such, in a manner similar to that noted in U.S. Patent

No. 5,003,558 discussed above performing this extra task, however, consumes valuable processing time, and reduces system efficiency. Moreover, by loading the transmit buffer with "dummy" ATM cells, overall data transport latency increases because such data must be flushed in serial fashion through the channel to the upstream transceiver, even when new transmit data is available from the operating system.

Accordingly, the commonly suggested techniques for handling latency in an ADSL software environment while maintaining a synchronous link are impractical, and, in many cases, inefficient.

SUMMARY OF THE INVENTION

An object of the present invention, therefore, is to provide an improved system and method for maintaining a continuous and uninterrupted ADSL data bit stream between an operating system implementing a downstream transceiver, and a remote upstream transmitter;

A further object of the present invention is to provide an improved ATM protocol system and method which is simpler to implement in an ADSL software transceiver;

A related object of the present invention is to provide an improved system and method for reducing overall data transport latency in a data path between an operating system implementing a downstream transceiver, and a remote upstream transmitter.

A further object of the present invention is to apply the above methods in any high-speed synchronous transmission systems which must include a source of asynchronous traffic transport.

A system of the present invention therefore eliminates latencies caused by asynchronous data transport requirements associated with a synchronous data channel, which, in a preferred embodiment, carries ADSL signals in accordance with known protocols and standards. The system first includes a logical data layer, which is coupled to the asynchronous operating system, which can be a personal computer. This logical layer receives data blocks corresponding to actual data to be transmitted by applications running on an asynchronously running operating system. These data blocks are converted into actual data logical blocks. A transmit data buffer is coupled

to the logical data layer, and stores the actual data logical block after it is processed by the logical data layer. A dummy data buffer is used for storing a dummy data logical block corresponding to a logical data block containing no actual operating system data, i.e., a fixed data pattern that can sent on the synchronous data link as fill data to maintain synchronization. A physical data layer is also coupled to the transmit data buffer, the dummy data buffer, and the synchronous data channel. The physical data layer converts the actual data logical blocks into actual data digital signals for transmission in the synchronous data channel. It also converts the dummy data logical blocks to dummy data digital signals for transmission in the synchronous data channel to maintain synchronization as noted. Thus, the physical data layer transmits real data digital signals to the synchronous data channel when there is an actual data logical block in the transmit data buffer and otherwise transmits the dummy data digital signals. The dummy data logical block is selected to be equal in size to a single actual data logical block to facilitate handling by the physical layer.

The advantages of this approach are many, and include the fact that the latency is reduced because dummy data is not stored in the transmit buffer, and the fact that the logical layer does not waste time storing such dummy data in the first place. Furthermore, the latency in the synchronous data channel is limited to be no more than the time required to transmit a single dummy data logical block. More importantly, it can be seen that the latency is substantially independent of any latency caused by the asynchronous operating system.

In a preferred embodiment, the latency reduction system is used within a software modem environment.

In this regard, the logical data layer is implemented as an ATM protocol layer, which has a transmit routine for converting the asynchronous data block into an actual logical data block corresponding to an ATM cell. Such protocol layer can be implemented in hardware, or preferably, as an ATM protocol routine executed by a processing device within the asynchronously operating computing system. The transmit portion (subroutine) of the ATM protocol routine is specifically configured, therefore, so that when no actual operating system data is available for transmission, it does load any data (or dummy data cells) into the transmit data buffer. The transmit portion of the ATM protocol routine is preferably activated or invoked whenever the transmit data buffer contains an amount of data less than a transmit threshold value (or

water mark).

Further in a preferred embodiment, the physical data layer is an ADSL physical layer routine executed by the processing device. Such physical layer can be implemented in dedicated front end transceiver hardware, or preferably as an ADSL physical data layer routine which is executed with a higher priority (or lower latency) than the ATM protocol routine. The ADSL physical layer transmit routine sends a dummy data digital signal when there is no data, but does not load such data from the transmit data buffer. At the end of such operation, it checks the transmit data buffer to determine if any actual data logic block should be converted and transmitted. If yes, it does not send any further dummy data, and goes on to send real data. This operational feature ensures the maximum 1 dummy cell maximum latency length.

A preferred embodiment of an ADSL transceiver implemented in accordance with the present invention includes the aforementioned latency reduction system, as well as a number of additional transmit and receive components. In particular, a downstream transceiver front end circuit is coupled to the physical data layer and converts the real data digital signals and the dummy data digital signals into real data analog signals and dummy data analog signals respectively for transmission through the synchronous channel to a second upstream transceiver. As part of this front end, a second transmit data buffer is coupled between the physical data layer and the downstream transceiver front end circuit for storing data corresponding to the real data digital signals and the dummy data digital signals. Such front end also includes a first receive data buffer coupled between the physical layer and the downstream transceiver front end circuit for storing data corresponding to received data digital signals from the upstream transceiver. In addition, a second receive data buffer is coupled between the physical data layer and the logical data layer for storing data corresponding to received data logical blocks from the upstream transceiver. This latter structure helps minimize latency on the receive side of the transmitter.

The latency reducing system of the present invention, including the physical layer and logical layer routines, can also be implemented in a computer program executable within the aforementioned operating system. Alternatively, the system can be embedded in silicon form such as in a programmed ROM or the like which can be executed by a dedicated hardware DSP.

A preferred method of transmitting data between a synchronous data channel

and an asynchronous operating system based on the present invention accomplishes this objective by generally performing the following steps: (a) determining if there is actual data to be transmitted by the asynchronous operating system; (b) converting any such actual data into an actual data logical block; and (c) buffering the actual data logical block; and (d) determining whether an actual data logical block has been buffered; and (e) when an actual data logical block has been buffered, converting the actual data logical block into actual data digital signals for transmission in the synchronous data channel; and when no actual data logical block has been buffered, converting a dummy data logical block to dummy data digital signals for transmission in the synchronous data channel.

As noted above, the actual logical data block preferably corresponds to an ATM formatted cell. Again, too, only actual data logic blocks are buffered, which reduces latency significantly. When the number of actual data logical blocks falls below a predetermined threshold value, steps (a) through (c) are repeated. Since only actual data is stored in the transmit buffer, the use of the water mark or threshold provides significant performance advantage because it now more accurately reflects transmit data status.

As also alluded to above, the aforementioned steps are preferably performed by various routines executed by a software modem. As such, these steps are performed by a number of routines executed by a processing device within the asynchronous computing system. Also, as noted earlier, the logical layer routine is executed with a lower priority than the physical layer routine. The same latency improvement advantages as outlined above are possible with the disclosed method therefore.

A method of implementing an ADSL transceiver, therefore, includes the aforementioned latency reducing process, as well as further necessary steps. These include, generally, a step (f): converting the real data digital signals and the dummy data digital signals into real data analog signals and dummy data analog signals respectively for transmission through the synchronous channel to a second upstream transceiver. Again, an additional step (g) can also be employed of buffering data corresponding to the real data digital signals and the dummy data digital signals. On the receiving side, the preferred method includes a step (h): buffering data corresponding to received data digital signals from the upstream transceiver. An additional step (i): buffering data corresponding to received data logical blocks from

the upstream transceiver is also executed.

Although the inventions are described below in a preferred embodiment involving an ADSL transceiver, it will be apparent to those skilled in the art the present invention would be beneficially used in many environments where it is necessary to minimize latencies in a real time data transmission path for non-real time traffic transport.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram illustrating an embodiment of a system implemented in accordance with the teachings of the present invention;

FIGs. 2A and 2B depicts in flow chart form the general method of operation of a ATM Protocol Layer and an ADSL Physical Layer of the present invention as identified in FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

A preferred embodiment of a system 100 of the present invention is illustrated in FIG. 1. With the exception of some of the details of the transmit buffer logic used in the present system, the other components shown in FIG. 1 are well-known ADSL transceiver circuits, and hence will not be explained in detail herein. System 100 is a downstream ADSL transceiver coupled through a channel 101 to an upstream transceiver 102. A continuous data stream is maintained in both a downstream and upstream direction between such transceivers. This is done so that synchronization is maintained, and overall data transport latency is minimized. An analog front end (AFE) 103 of transceiver 100 includes conventional telephone line interface, an optional splitter, various filters, and an analog to digital converter circuit for converting a received ADSL signal to a series of digital samples. Corresponding circuitry on the transmit side converts a series of digital samples into analog data signals for transmission through channel 101. The specifics of AFE 103 are well-known in the art, and as they are not material to the present invention, a detailed explanation of the same is not necessary to an understanding of the present teachings.

An ADSL Physical Layer 110 is coupled to AFE 103 through a first receive buffer 106. As mentioned above, ADSL Physical Layer 110 is preferably an ISR implemented on a personal computing system using the Microsoft Windows operating system. This ISR, as is apparent, performs both receive and transmit functions in receive and transmit routines respectively. Generally speaking, both of these routines have a high priority and are responsible for, among other things, demodulating/modulating the received DMT digital samples and converting them into a received/transmit data stream.

The other side of ADSL Physical Layer 110 is coupled through a second receiver buffer 116 to ATM Protocol layer 120. As noted earlier, ATM protocol layer 120 is preferably a DPC implemented on a personal computing system using the

Microsoft Windows operating system. The functions and operations performed by ATM protocol layer 120 include generally, among other things, conversion of received ATM data cells into Internet Protocol (IP) packets, which can be handled by IP applications within the computing system, and conversely, conversion of any transmit data from such applications into ATM cells before ADSL Physical layer 110. This routine (including a receive and transmit portion) has a lower priority (or higher latency) than the routines associated with ADSL Physical Layer 110. Second receiver buffer 116 preferably includes a water mark (data receive threshold) 117, which is set to a value which takes into consideration a variety of data path and transceiver considerations, including expected operating system latencies, the size of buffer 116, etc. Accordingly, such value will vary from application to application, but in general, such value is set to a point usually near an "empty" buffer condition so that data can be continuously loaded without overflow when the system is busy and the receive sub-routines associated with ATM Protocol Layer cannot be activated. When a data level in buffer 116 goes above water mark level 117, the receiver part of the ATM protocol layer software routine is triggered by the host system. This routine removes data in the buffer 116 until its cell occupancy level falls below the water mark, or until such routine is interrupted by a higher priority task. Note that, as indicated with the dotted lines in FIG. 1, all the data flow up until this point involves interfaces that handle a time sensitive (synchronous) bit stream. ATM protocol layer 120 is also interfaced to an asynchronous communications path in the operating system and/or other applications 125 within a host computing system. As is apparent from FIG. 1, this is also the last leg of the receive side data link to the upstream transceiver 101. From the perspective of the upstream transceiver, it is imperative, of course, that the entire receive leg of the data link operate in a synchronous manner, and the aforementioned configuration discussed above can accomplish this objective in an ADSL transceiver 100 with minimal latency problems.

On the first leg of the transmit side, a transmit portion (routine) of ATM protocol layer 120 converts asynchronous input data traffic from the operating system and/or other applications into ATM cells. These ATM cells are then loaded into a second transmit buffer 115. As with second receiver buffer 116, second transmit buffer preferably includes a water mark 118, which is set to a value which takes into consideration a variety of data path and transceiver considerations, including expected

operating system latencies, the size of buffer 115, etc. Accordingly, such value will vary from application to application, but in general, such value is set to a point usually near a "full" buffer condition so that data is continuously loaded and emptied when there is activity on the transmit side. When a data level in buffer 115 goes below the water mark level, this triggers the transmit portion of ATM protocol layer 120, which adds cells to the buffer until the cell occupancy goes above water mark level 118, or until such routine is interrupted by a higher priority task. The data from the ATM cells in second transmit buffer 115 is modulated by a transmit portion (routine) of ADSL Physical Layer 110 into digital data samples. Such digital samples are then communicated to a first transmit buffer 105, and are retrieved by AFE 103 where they are further converted into an analog data signal that is transmitted through channel 101 back to transceiver 102.

The aforementioned description is fairly typical for implementation in an ADSL software modem. The specifics of such implementation of first receiver buffer 106, first transmitter buffer 105, second receiver buffer 116, second transmit buffer 115, AFE 103, and ADSL Physical Layer 110 are again not important to the present invention, and therefore any combination of computing hardware and software routines can be employed which can perform the tasks required of such transceiver elements. In a preferred embodiment, both second receiver buffer 116 and second transmit buffer 115 are implemented as software FIFOs, meaning they are set up and maintained within a regular system memory by ATM Protocol Layer 120 and/or ADSL Physical Layer 110. This approach has an advantage over pure hardware FIFOs, however, in that such structures can be dynamically re-sized as necessary, based on receive and transmit requirements, system performance, etc. Furthermore, a buffer pointer indicating the starting item of data in a data buffer can be reset as needed, which avoids the latency issues associated with a hardware FIFO where, if "idle" data is present in the queue before real data, such idle data must still be transmitted to flush the buffer.

The important distinction is that the present invention overcomes the latency problems of the prior art through the use of an improved ATM protocol layer 120, and a "dummy" cell buffer 130 as now explained more fully. As noted earlier, at many times, there is no real data traffic on the transmit side coming from applications 125; in such cases, the transmit portion of ATM protocol layer 120 must insert "dummy"

cells into second transmit buffer 115. This is because, as also explained above, an overall constant data stream bit rate meeting the ADSL standard must be maintained on this side of ADSL transceiver 100. In other words, the return leg of the ADSL link must be kept synchronous as well, despite the fact that there is an asynchronous data source at one end. These dummy cells are inserted into the bit stream, but are discarded at the other end of the data link by upstream transceiver 102 because they carry no information. Unlike other systems, however, the transmit portion of ATM protocol layer 120 of the present invention does not load second transmit buffer 115 with dummy cells, even when there is no data traffic forthcoming from applications 125. Instead, the transmit portion of ATM protocol layer 120 only loads actual data cells to second transmit buffer 115. Accordingly, second transmit buffer 115 is never loaded with dummy cells, and only contains actual transmit data. To handle the problem of stuffing the bit stream with dummy cells to maintain synchronization, a separate dummy buffer 130 is employed. This dummy buffer contains a predefined cell pattern for the dummy cell that would otherwise be generated, retrieved or transmitted by the transmit subroutine portion of ATM protocol layer 120. Like second transmit buffer 115, dummy buffer 130 is also coupled to ADSL Physical Layer 110, and therefore can provide the dummy cell pattern data as required during a transmit operation. As with second transmit buffer 115, dummy buffer can be implemented as a software structure in system memory of arbitrary size, or in hardware since the cell pattern data is fixed. It is conceivable, of course, that dummy buffer can contain patterns other than dummy cells which may be fixed data patterns that must be transmitted to an upstream transceiver during portions of a data transmission. Again, as with other systems which utilize a transmit buffer "water mark," (or transmit data threshold) a transmit portion of ATM Protocol Layer 120 can be activated when transmit data buffer 115 falls below the transmit water mark.

FIGs. 2A and 2B are flow chart forms of the operation of an ATM Protocol Layer 120 routine, and an ADSL Physical layer 110 routine, respectively, as implemented in a preferred embodiment of the present invention. For the ATM Protocol Layer 120 transmit routine shown in FIG. 2A, the following steps are executed: first, at step 205, the routine is invoked when the cell occupancy level in second transmit data buffer 215 falling below a water mark level value 218. Then, at step 210, an examination is made to determine if there is additional data from

applications 225 that needs to be transmitted. If not, the routine ends at step 215; i.e. no dummy data blocks (ATM sized dummy cells) are loaded into second transmit data buffer 215. If there is data that needs to be sent, it is processed at step 220 using any one of a number of well-known techniques so that data is converted into a logical data block (i.e. ATM cells) of any suitable length and format for the particular data link.

Thus, second transmit data buffer 115 only contains actual logical data blocks to be transmitted, and not dummy cell data, which means that latency is reduced and system performance is improved. This can be seen from a simple example; in a conventional approach, if dummy cells are loaded into second transmit data buffer 115, they will fill such buffer, causing a data level to rise, and potentially exceeding the water mark level. This means that ATM protocol routine 120 will not be invoked, even though there is no real data in the transmit queue. In fact, it is conceivable that second transmit data buffer 115 may contain no real data, and that a large amount of time will be spent flushing this buffer of dummy cells before real data can be processed by ADSL Physical layer 110. Thus, the present invention significantly enhances the value of a transmit buffer data water mark in a synchronous data link that includes "dummy" data cells as data stream "filler," because such water marks, when used with a buffer containing only real data, can now accurately represent the status of the amount of transmit data ready for transmission.

In FIG. 2B, the operation of transmit portion (routine) of ADSL Physical Layer 110 is shown. At step 225, the routine is invoked by the periodic transmit opportunities of ADSL modulated symbols. In T1.413 and G.992 standards, the period for each invocation is approximately 250 μsec. The routine then continues at step 230 to read data from whichever of second transmit data buffer 115 or dummy cell buffer 130 is designated as the "current" buffer, until reaching the end of a current ATM cell. Then, if at step 235 dummy cell buffer 130 is the current buffer, at step 240 it will read such dummy cell, and, at the end of reading such cell, check second transmit data buffer 115 at step 242 to see if contains any real transmitted data cells from applications 225. This is done by setting a buffer pointer to the head of second transmit data buffer 115. If there is any such data, ADSL Physical Layer 110 then switches at step 245 to reading data from second transmit data buffer 115, and designates such buffer as the current buffer. If not, it sets a new buffer pointer to the start of the dummy buffer, and continues to read from dummy cell buffer 130 as

before.

On the other hand, if at step 235 second transmit data buffer 115 is the current buffer, it will continue reading from there at step 255 until it reaches the end of such buffer. Once it reaches the end of such buffer, it will then switch at step 260 to reading from dummy buffer 130, and designates such buffer as the current buffer.

It can be seen from the above description that at any moment in time, the worst case maximum latency, from a data transmit perspective, is at most one ATM cell in duration. The best case minimum latency, conversely, is 0. Thus, the average expected latency with the present invention is only half of an ATM cell size. Moreover, such latency is completely independent of the operating system latency, which is a significant benefit for an ADSL based software modem, because of the wide variation in performance and latency of computing systems incorporating the same. Accordingly, the present invention can be advantageously employed in any synchronous transmission link which utilizes a predefined "idle" signal pattern to compensate for sources of asynchronous data transport.

Although the present invention has been described in terms of a preferred embodiment, it will be apparent to those skilled in the art that many alterations and modifications may be made to such embodiments without departing from the teachings of the present invention. It will also be apparent to those skilled in the art that for purposes of the present discussion, the block diagram of the present invention has been simplified. The microcode and software routines executed by the host processor to effectuate the inventive methods may be embodied in various forms, including in a permanent magnetic media, a non-volatile ROM, a CD-ROM, or any other suitable machine-readable format. Accordingly, it is intended that the all such alterations and modifications be included within the scope and spirit of the invention as defined by the following claims.

What is claimed is:

1. A system for transmitting data between a synchronous data channel and an asynchronous operating system, said system comprising:

a logical data layer coupled to the asynchronous operating system, said logical data layer being capable of receiving a data block corresponding to actual data to be transmitted by the asynchronous operating system, and further being capable of converting said data block into an actual data logical block; and

a transmit data buffer coupled to said logical data layer for storing said actual data logical block after it is processed by said logical data layer; and

a dummy data buffer for storing a dummy data logical block corresponding to a logical data block containing no actual operating system data; and

a physical data layer coupled to said transmit data buffer, said dummy data buffer, and the synchronous data channel, said physical data layer being capable of converting said actual data logical block into actual data digital signals for transmission in said synchronous data channel, and said physical data layer further being capable of converting said dummy data logical block to dummy data digital signals for transmission in said synchronous data channel; and

wherein said physical data layer transmits said real data digital signals to the synchronous data channel when said transmit data buffer contains an actual data logical block, and otherwise transmits said dummy data digital signals.

2. The system of claim 1, further wherein said logical data layer converts said asynchronous data block into an actual logical data block corresponding to an ATM cell.

3. The system of claim 1, further wherein said logical data layer is configured such that when no actual operating system data is available for transmission, said logical data layer does not load any actual data logical blocks in said transmit data buffer.

4. The system of claim 1, further wherein said transmit data buffer includes a data transmit threshold value, such that when said transmit data buffer contains an amount of data less than said data transmit threshold value, said logical data layer is activated to determine if additional actual operating system data is available for transmission.

5. The system of claim 1, wherein said dummy data logical block is the same size as a single actual data logical block.

6. The system of claim 1, wherein said logical data layer is an ATM protocol routine executed by a processing device within a computing system.

7. The system of claim 6, wherein said physical data layer is an ADSL physical layer routine executed by said processing device.

8. The system of claim 7, further wherein said ADSL physical data layer routine is executed with a higher operating system priority or lower latency than said ATM protocol routine.

9. The system of claim 7, wherein after sending a dummy data digital signal, said ADSL physical data layer routine checks said transmit data buffer to determine if any actual data logic block should be converted and transmitted.

10. The system of claim 1, further wherein a latency in said synchronous channel is no greater than a time required to transmit said dummy data logical block.

11. The system of claim 1, further wherein a latency in said synchronous channel is substantially independent of any latency inherent in said asynchronous operating system.

12. The system of claim 1, further including a downstream transceiver front end circuit coupled to said physical data layer and being capable of converting said real data digital signals and said dummy data digital signals into real data analog signals and dummy data analog signals respectively for transmission through the synchronous channel to a second upstream transceiver.

13. The system of claim 12, further including a second transmit data buffer coupled between said physical data layer and said downstream transceiver front end circuit for storing data corresponding to said real data digital signals and said dummy data digital signals.

14. The system of claim 13, further including a first receive data buffer coupled between said physical layer and said downstream transceiver front end circuit for storing data corresponding to received data digital signals from said upstream transceiver.

15. The system of claim 14, further including a second receive data buffer coupled between said physical data layer and said logical data layer for storing data corresponding to received data logical blocks from said upstream transceiver.

16. The system of claim 1, wherein said real time data channel is a data link transmitting data symbols in accordance with ADSL transmission protocol standards.

17. A machine executable program for transmitting data between a synchronously operated high data channel and an asynchronously operated operating system, said program comprising:

a first priority routine, said first priority routine being configured such that:

(a) said first priority routine determines whether there is actual data to be transmitted by such operating system; and

(b) when actual data is to be transmitted:

[1] said first priority routine converts any such actual data into an actual data logical block; and

[2] said first priority routine buffers said actual data logical block; and

[c] when no actual data is to be transmitted, said first priority routine performs no further data transmission operations;

a second priority routine, said second priority routine being configured such that:

(a) when actual data is to be transmitted said second priority routine converts said actual data logical block into actual data digital signals for transmission in the high speed data channel; and

(b) (b) when no actual data is to be transmitted, said second priority routine alternatively converts a dummy data logical block to dummy data digital signals for transmission in said real time data channel.

wherein latencies associated with the operating system transferring data to the data channel are substantially eliminated.

18. The program of claim 17, wherein said first routine converts said actual data into ATM cells.

19. The program of claim 17, wherein said second routine converts said actual data logical block and said dummy data logical block into discrete multi-tone modulated signals compatible with an ADSL protocol used in said high speed channel.

20. The program of claim 17, further wherein said first priority routine is activated when a number of actual data logic blocks to be transmitted falls below a predetermined threshold value.

21. The program of claim 17, further wherein said second routine has a higher priority for execution within the operating system than said first routine.

22. The program of claim 17, further wherein a latency in said high speed channel is no greater than a time required to transmit said dummy data logical block.

23. The program of claim 22, further wherein a latency in said high speed channel is substantially independent of any latency caused by said operating system.

24. A method of transmitting data between a synchronous data channel and an asynchronous operating system, said method comprising the steps of:

(a) determining if there is actual data to be transmitted by the asynchronous operating system;

(b) converting any such actual data into an actual data logical block; and

(c) buffering said actual data logical block; and

(d) determining whether an actual data logical block has been buffered; and

(e) [i] when an actual data logical block has been buffered, converting said actual data logical block into actual data digital signals for transmission in said synchronous data channel; and

[ii] when no actual data logical block has been buffered, converting a dummy data logical block to dummy data digital signals for transmission in said Synchronous data channel.

25. The method of claim 24 wherein actual logical data block corresponds to an ATM cell.

26. The method of claim 24, further wherein only actual data logic blocks are buffered.

27. The method of claim 24, further wherein a plurality of said actual data logical blocks are buffered; and further wherein when a number of said plurality of actual data logical blocks falls below a predetermined threshold value, steps (a) through (c) are repeated.

28. The method of claim 24, wherein said dummy data logical block is the same size as a single actual data logical block.

29. The method of claim 24, wherein steps (a) through (c) are performed by a first routine executed by a processing device within a computing system.

30. The method of claim 29, wherein steps (d) and (e) are performed by a second routine executed by said processing device.

31. The method of claim 30, further wherein said second routine is executed with a higher priority or lower latency than said first routine.

32. The method of claim 29, wherein after sending a dummy data digital signal at step (e)[ii], step (d) is repeated, and if no actual data logic block exists, step (e)[ii] is repeated.

33. The method of claim 24, further wherein a latency in said synchronous channel is no greater than a time required to transmit said dummy data logical block.

34. The method of claim 24, further wherein a latency in said synchronous channel is substantially independent of any latency caused by said asynchronous time operating system.

35. The method of claim 24, further including a step (f): converting said real data digital signals and said dummy data digital signals into real data analog signals and dummy data analog signals respectively for transmission through the synchronous channel to a second upstream transceiver.

36. The method of claim 35, further including a step (g): buffering data corresponding to said real data digital signals and said dummy data digital signals.

37. The method of claim 36, further including a step (h): buffering data corresponding to received data digital signals from said upstream transceiver.

38. The method of claim 37, further including a step (i): buffering data corresponding to received data logical blocks from said upstream transceiver.

39. The method of claim of claim 24, wherein said synchronous data channel is a data link transmitting data symbols in accordance with ADSL transmission protocol standards.

40. A method of reducing latency in a software transceiver between an operating system and a high speed data channel both coupled to such transceiver, said method comprising the steps of:

(a) executing a first priority routine running in the operating system to determine if there is actual data to be transmitted by such operating system;

(b) [i] when actual data is to be transmitted said first priority routine:

[1] converts any such actual data into an actual data logical block;

[2] buffers said actual data logical block; and

[ii] when no actual data is to be transmitted, said first priority routine performs no further data transmission operations;

(c) executing a second priority routine running in the operating system such that:

[i] said second priority routine converts said actual data logical block into actual data digital signals for transmission in the high speed data channel;

[ii] said second priority routine converts a dummy data logical block to dummy data digital signals for transmission in said real time data channel to maintain a continuous data stream in said high speed data channel.

wherein latencies associated with the operating system transferring data to the data channel are substantially eliminated.

41. The method of claim 40, wherein said actual data logical blocks include ATM cells.

42. The method of claim 40, wherein said actual data digital signals are discrete multi-tone modulated signals compatible with an ADSL protocol used in the channel.

43. The method of claim 40, further wherein said first priority routine is activated when a number of actual data logic blocks to be transmitted falls below a predetermined threshold value.

44. The method of claim 40, further wherein said second routine is executed with a higher priority than said first routine.

45. The method of claim 40, further wherein a latency in said high speed channel is no greater than a time required to transmit said dummy data logical block.

46. The method of claim 45, further wherein a latency in said high speed channel is substantially independent of any latency associated with said operating system.

FIG. 1

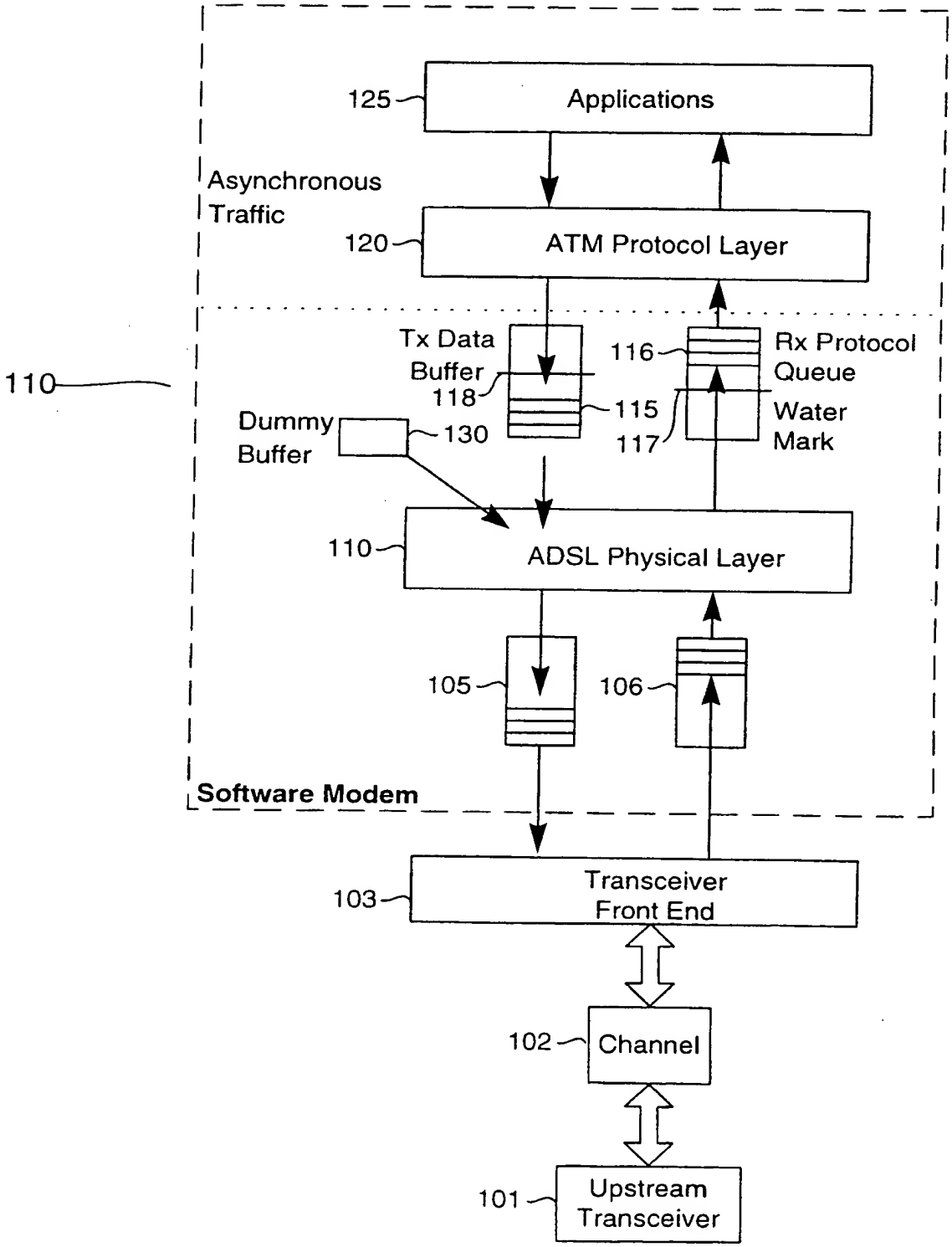


FIG. 2A

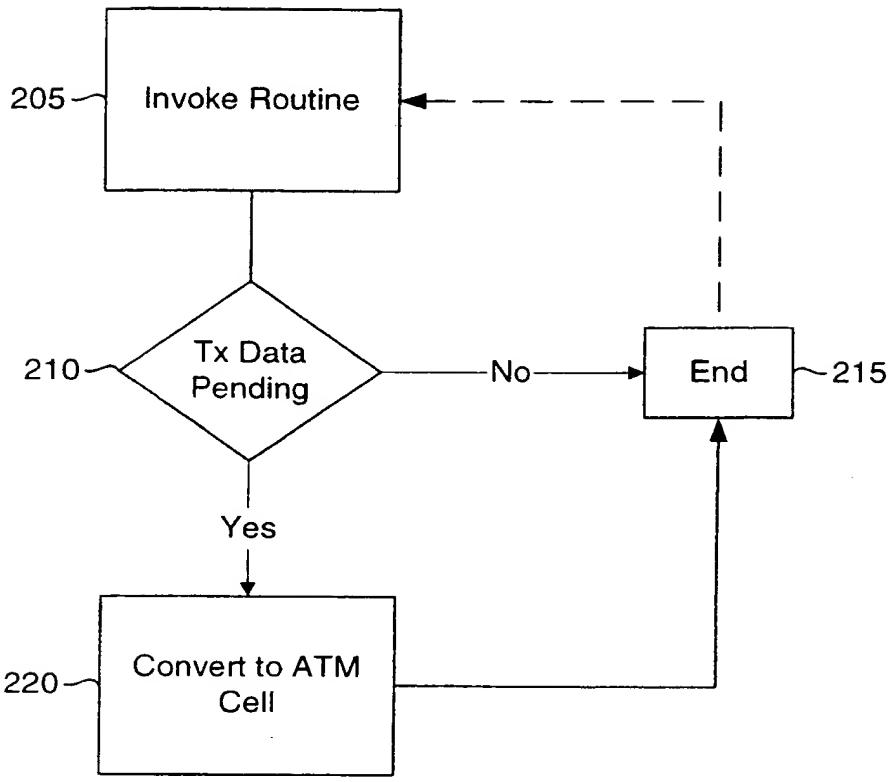
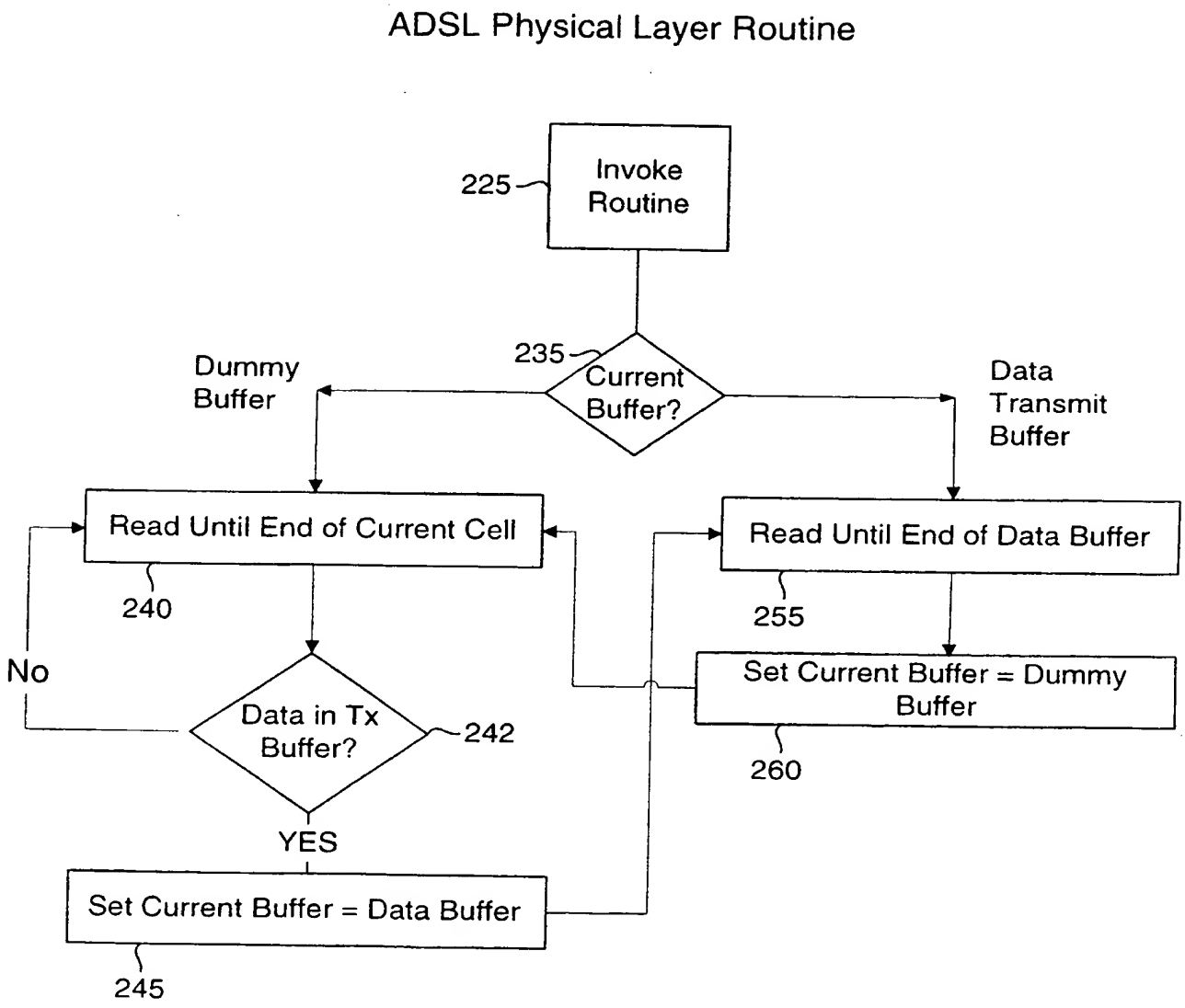


FIG. 2B



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/26944

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H04L 12/28; H04J 3/16, 3/24
US CL : 370/395,466,474
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 370/282,352,353,354,395,397,466,469,474

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ------ Y	US 5,541,926 A (SAITO ET AL) 30 JULY 1996 (30.07.96), column 6, lines 50-67, column 7, lines 1-67, column 8, lines 8-15, column 9, lines 38-59 and Figures 3,4,5,8,16,17 and 20.	1-2,4-6, 9-11, 17-18, 20-26, 28-34, 38,40-41, 43,45-46 --------- 12 and 35
Y,P	US 5,933,426 A (MOTOORI) 03 August 1999 (03.08.99), column 11, lines 7-21.	12 and 35.

☐ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

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Date of the actual completion of the international search
10 FEBRUARY 2000

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INTERNATIONAL SEARCH REPORT

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